IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant: William A. Harris

Title: PRECISION PHASE GENERATOR

Docket No.: H26054US (256.058US1)
Filed: December 29, 2000
Examiner: Cassandra F. Cox

Serial No.: 09/751,610
Due Date: September 7, 2004
Group Art Unit: 2816

Mail Stop Appeal Brief--Patents
Commissioner for Patents
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Gina Uphus
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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)

PATENT

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APPELLANTS' BRIEF ON APPEAL

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on July 7, 2004, from the Final Rejection of claims 1-3, 20-24, 26-29, 31-37, 39-45, 47 and 48 of the above-identified application, as set forth in the Final Office Action dated April 7, 2004.

This Appeal Brief is filed in triplicate. The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of 330.00 which represents the requisite fee set forth in 37 C.F.R. § 117. The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims.

APPELLANTS' BRIEF ON APPEAL

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, HONEYWELL INTERNATIONAL INC.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

Claims 1-3, 20-24, 26-29, 31-37, 39-45, 47 and 48 are pending in the application and have all been finally rejected. The rejected claims 1-3, 20-24, 26-29, 31-37, 39-45, 47 and 48 are the subject of the present appeal.

4. STATUS OF AMENDMENTS

No Amendment has been filed by the applicant subsequent to the Final Office Action dated 7 April 2004.

5. SUMMARY OF THE INVENTION

The MPEP indicates that it is preferable to read the appealed claims on the specification and any drawing.[1] Representative of the appealed claims, appealed claim 40 is reproduced herein with reference numerals added to indicate the corresponding elements in the Figures that are described in the specification.

Appealed claim 40 recites a method of generating multiple output clock signals comprising: applying an input clock signal having a frequency F_0 to a signal input 104, 202 of a phase lock loop circuit 102; applying a feedback signal to an error input 106, 206 of the phase

1 MPEP 1206.

lock loop circuit 102; generating an output signal 108, 217 having a frequency $2NF_0$ from the phase lock loop circuit 102 wherein N is a positive integer; coupling the output signal 108, 217 having the frequency $2NF_0$ from the phase lock loop circuit 102 to a clock input of each JK flip-flop 220, 222, 224, 226 of a Johnson counter 104, the Johnson counter 104 comprising N JK flip-flops including an input JK flip-flop 220, an output JK flip-flop 226, and a plurality of middle JK flip-flops 222, 224, each JK flip-flop having a J input, a K input, the clock input, a Q output, and a complemented Q output, each middle JK flip-flop 222, 224 and the output JK flip-flop 226 having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop 220 being coupled to the complemented Q output of the output JK flip-flop 226, the K input of the input JK flip-flop 220 being coupled to the Q output of the output JK flip-flop 226; generating the feedback signal in the Johnson counter 104 in response to the output signal 108, 217 having the frequency $2NF_0$ from the phase lock loop circuit 102; and generating an output clock signal 228, 230, 232, 234 from at least two of the N JK flip-flops 220, 222, 224, 226 of the Johnson counter 104, each output clock signal having a phase displaced from a phase of each other output clock signal by at least $360/2N°$.

6. ISSUE PRESENTED FOR REVIEW

Whether claims 1-3, 20-24, 26-29, 31-37, 39-45, 47 and 48 are unpatentable under 35 USC § 103(a) over Li et al. (U.S. Patent No. 5,058,132, Li) in view of Epstein (U.S. Patent No. 4,093,870).

7. GROUPING OF CLAIMS

Claims 1-3, 20-24, 26-29, 31-37, 39-45, 47 and 48 stand together for purposes of this appeal.

Appellant does not make any admission that any claim may not be argued in another forum as independently patentable from any other claim. Additionally, Appellant's grouping of claims above is provided for the purposes of this Appeal Brief only.

8. ARGUMENT

The Applicable Law

All of the pending claims were rejected under 35 U.S.C. §103(a):

> "A patent may not be obtained...if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." [2]

The MPEP requires a suggestion and a reasonable expectation of success for a rejection under 35 USC §103:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."[3]

A Federal Circuit opinion states that the suggestion or motivation to combine references and the reasonable expectation of success must both be found in the prior art.[4]

Multiple Federal Circuit decisions emphasize the need for the PTO to furnish evidence in support of claim rejections. For example, the Federal Circuit addressed citation of "basic knowledge and common sense" in rejections in *In re Zurko*:

> "With respect to core factual findings in a determination of patentability, however, the Board [Board of Patent Appeals and Interferences] cannot simply reach conclusions based

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2 35 U.S.C. §103(a).
3 MPEP 2143.
4 MPEP 2143 citing *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).

> on its own understanding or experience – or on its assessment of what would be basic knowledge or common sense. Rather, the Board must point to some concrete evidence in the record in support of these findings."[5]

The Federal Circuit has particularly emphasized the need for the PTO to furnish evidence in support of claim rejections under 35 USC § 103 in *In re Lee*:

> "When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness.....The factual inquiry whether to combine references must be thorough and searching....It must be based on objective evidence of record."[6]

The Federal Circuit stated that the "need for specificity pervades this authority" requiring a teaching, motivation, or suggestion to select and combine references.[7] The Federal Circuit has expressed this need for specificity in several cases:

> "[T]he best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.....the showing must be clear and particular."[8]
>
> "[E]ven when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination."[9]
>
> "[P]articular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed."[10]

Rejection

Claims 1-3, 20-24, 26-29, 31-37, 39-45, 47 and 48 were rejected under 35 USC §103(a) as being unpatentable over Li in view of Epstein.

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5 *In re Zurko*, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001).
6 *In re Lee*, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).
7 *In re Lee*, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).
8 *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).
9 *In re Rouffet,* 47 USPQ2d 1453, 1459 (Fed. Cir. 1998).
10 *In re Kotzab,* 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

Claims 1-3, 20-24, 26-29, 31-37, 39-45, 47 and 48 stand together for purposes of this appeal. The appellant respectfully submits that the final Office Action has not presented evidence of a suggestion or motivation to combine Li and Epstein or a reasonable expectation of success of this combination as required by *In re Vaeck* and *In re Lee*.

Li relates to a clock distribution system and shows a circuit called a Johnson counter 114 in Figure 2. Epstein relates to an apparatus for testing reflexes and shows a circuit called a Johnson counter 54 in Figure 4. Epstein's Johnson counter 54 has only three JK flip-flops. Neither Li nor Epstein show a Johnson counter comprising an input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops as is recited in the appealed independent claims 1, 20, 32, and 40. Therefore, even as combined, Li and Epstein do not show the claimed invention. In addition, there is no evidence of a suggestion or motivation to modify Epstein or to combine Li and Epstein.

The final Office Action proposed that it would have been obvious to add more flip-flops to Epstein stating that "it is considered to be well known that you could have any number of middle flip-flops depending on the requirements of the circuit."[11] This is not so because adding flip-flops would produce a different counter output for each added flip-flop. It would not be obvious to substitute one for another without a clear and particular teaching as required by *In re Dembiczak*. The Office Action did not cite a prior art source of the above quote in modifying Epstein. The Office Action has not presented evidence from the prior art of a teaching or motivation to modify Epstein as is required by *In re Vaeck* and *In re Lee*.

The final Office Action stated that it would have been obvious to combine Li and Epstein "Since, Li does not disclose the particular construction of the Johnson counter any Johnson counter could be used and the Johnson counter of Epstein is one example."[12] This is not so simply because of the variety of circuits called Johnson counters. For example, Li, Epstein, and Moreau (U.S. Patent No. 4,282,493, of record) each refer to a different circuit as a Johnson

11 Final Office Action, page 3.

counter. Each of the circuits shown in Li, Epstein, and Moreau would produce a different counter output. It would not be obvious to substitute one for another without a clear and particular teaching as required by *In re Dembiczak*. The final Office Action did not cite a prior art source of the above quote in combining Epstein and Li. The final Office Action has not presented evidence from the prior art of a teaching or motivation to combine Li and Epstein as is required by *In re Vaeck* and *In re Lee*.

The final Office Action has also not presented evidence a reasonable expectation of success of this combination of Li and Epstein as required by *In re Vaeck* and *In re Lee*.

The applicant respectfully submits that a *prima facie* case of obviousness against claims 1-3, 20-24, 26-29, 31-37, 39-45, 47 and 48 has not been established in the final Office Action. Reversal of the rejection of claims 1-3, 20-24, 26-29, 31-37, 39-45, 47 and 48 under 35 U.S.C. § 103 is respectfully requested.

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12 Final Office Action, page 3.

9. SUMMARY

For the foregoing reasons, the appellant respectfully submits that the final rejection of claims 1-3, 20-24, 26-29, 31-37, 39-45, 47 and 48 under 35 U.S.C. § 103 was erroneous. Reversal of this rejection is respectfully requested, as well as the allowance of all the rejected claims.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

WILLIAM A. HARRIS

By his Representatives,

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Date 7 September 2004 By _____

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Gina M. Uphus
Name

_____
Signature

APPENDIX

The Claims on Appeal

1. (Previously Presented) A circuit for dividing an input clock signal into N clock signals having a relative phase separation of 360°/2N, where N is a positive integer, the circuit comprising:

a phase lock loop circuit receiving an input signal having a frequency F_0 and providing an output signal having a frequency $2NF_0$;

a Johnson counter having N JK flip-flops connected to receive as an input the output signal of the phase lock loop circuit and providing an output signal as an error signal to the phase lock loop circuit, said Johnson counter comprising an input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops, each JK flip-flop having a J input, a K input, a clock input coupled to receive the output signal having the frequency $2NF_0$ from the phase lock loop circuit, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, and the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop; and

said Johnson counter also being connected for providing at least two output signals from at least two of the N JK flip-flops of the Johnson counter as clock signals each having a phase displaced from the phase of the other 360/2N°.

2. (Original) The circuit of claim 1 wherein N =4.

3. (Original) The circuit of claim 1 wherein N=8.

4-19. (Canceled)

20. (Previously Presented) A method for generating at least two clock signals displaced from each other by a predetermined phase shift of 360°/2N, where N is a positive integer, the method comprising:

applying a clock signal to a signal input of a phase lock loop circuit at a desired clock frequency;

applying a feedback signal to a second input of the phase lock loop circuit;

generating an output signal of the phase lock loop circuit having a frequency of $2NF_0$;

coupling the output signal of the phase lock loop circuit to a clock input of each JK flip-flop of a Johnson counter to provide the feedback signal to the second input of the phase lock loop circuit having a frequency corresponding to the frequency of the output signal of the phase lock loop circuit divided by 2N, the Johnson counter comprising N JK flip-flops including an input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops, each JK flip-flop having a J input, a K input, the clock input, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop; and

coupling outputs of the JK flip-flops of the Johnson counter for use as phase shifted clock outputs.

21. (Original) The method of claim 20 wherein N =4.

22. (Previously Presented) The circuit of claim 1 wherein the Johnson counter is coupled to provide a clock signal from each of the N JK flip-flops in response to the output signal having the frequency $2NF_0$, the error signal being one of the clock signals, the N clock signals having a relative phase separation of at least 360°/2N and each clock signal having a frequency F_0.

23. (Previously Presented) The circuit of claim 1 wherein the error signal and each clock signal has a frequency F_0.

24. (Previously Presented) The circuit of claim 1 wherein the phase lock loop circuit comprises:

a phase detector coupled to receive and compare the input signal having the frequency F_0 and the error signal from the Johnson counter and to provide an output signal corresponding to a phase difference between the input signal having the frequency F_0 and the error signal;

a low pass filter and a gain stage coupled to receive the output signal from the phase detector and to produce a control signal;

a voltage controlled oscillator coupled to the low pass filter and the gain stage to receive the control signal and coupled to the Johnson counter to produce the output signal having the frequency $2NF_0$ in response to the control signal.

25. (Canceled)

26. (Previously Presented) The circuit of claim 1 wherein each Q output and each complemented Q output of each JK flip-flop is coupled to provide a clock signal, the 2N clock signals having a relative phase separation of 360°/2N, and each clock signal having a frequency F_0.

27. (Previously Presented) The method of claim 20 wherein the feedback signal is one of the clock outputs, the clock outputs having a relative phase separation of at least 360°/2N and each clock output having a frequency F_0.

28. (Previously Presented) The method of claim 20, further comprising generating the feedback signal and each clock output with a frequency F_0.

29. (Previously Presented) The method of claim 20 wherein generating an output signal of the phase lock loop circuit comprises:

comparing the clock signal at the signal input and the feedback signal in a phase detector;

generating an output signal from the phase detector corresponding to a phase difference between the clock signal at the signal input and the feedback signal;

generating a control signal in a low pass filter and a gain stage in response to the output signal from the phase detector; and

generating the output signal of the phase lock loop circuit in response to the control signal in a voltage controlled oscillator coupled to the low pass filter and the gain stage.

30. (Canceled)

31. (Previously Presented) The method of claim 20, further comprising:

generating a clock output from each Q output and each complemented Q output of each JK flip-flop of the Johnson counter, the 2N clock outputs having a relative phase separation of 360°/2N, and each clock output having a frequency F_0.

32. (Previously Presented) A circuit to divide an input signal into multiple output clock signals, the circuit comprising:

a phase lock loop circuit coupled to receive an input signal having a frequency F_0 and coupled to provide an output signal having a frequency $2NF_0$, wherein N is a positive integer; and

a Johnson counter having N JK flip-flops coupled to receive as an input the output signal of the phase lock loop circuit and coupled to provide an output signal as an error signal to the phase lock loop circuit, the Johnson counter also being coupled to provide at least two output signals from at least two of the N JK flip-flops of the Johnson counter as output clock signals, each output clock signal having a phase displaced from a phase of each other output clock signal by at least 360/2N°, the Johnson counter comprising an input JK flip-flop, an output JK flip-flop,

and a plurality of middle JK flip-flops, each JK flip-flop having a J input, a K input, a clock input coupled to receive the output signal having the frequency $2NF_0$ from the phase lock loop circuit, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, and the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop.

33. (Previously Presented) The circuit of claim 32 wherein N is 4.

34. (Previously Presented) The circuit of claim 32 wherein N is 8.

35. (Previously Presented) The circuit of claim 32 wherein the Johnson counter is coupled to provide an output clock signal from each of the N JK flip-flops in response to the output signal having the frequency $2NF_0$, the error signal being one of the output clock signals, the N output clock signals having a relative phase separation of at least 360°/2N and each output clock signal having a frequency F_0.

36. (Previously Presented) The circuit of claim 32 wherein the error signal and each output clock signal has a frequency F_0.

37. (Previously Presented) The circuit of claim 32 wherein the phase lock loop circuit comprises:

a phase detector coupled to receive and compare the input signal having the frequency F_0 and the error signal from the Johnson counter and to provide an output signal corresponding to a phase difference between the input signal having the frequency F_0 and the error signal;

a low pass filter and a gain stage coupled to receive the output signal from the phase detector and to produce a control signal;

a voltage controlled oscillator coupled to the low pass filter and the gain stage to receive the control signal and coupled to the Johnson counter to produce the output signal having the frequency $2NF_0$ in response to the control signal.

38. (Canceled)

39. (Previously Presented) The circuit of claim 32 wherein each Q output and each complemented Q output of each JK flip-flop is coupled to provide an output clock signal, the 2N output clock signals having a relative phase separation of 360°/2N, and each output clock signal having a frequency F_0.

40. (Previously Presented) A method of generating multiple output clock signals comprising:

applying an input clock signal having a frequency F_0 to a signal input of a phase lock loop circuit;

applying a feedback signal to an error input of the phase lock loop circuit;

generating an output signal having a frequency $2NF_0$ from the phase lock loop circuit wherein N is a positive integer;

coupling the output signal having the frequency $2NF_0$ from the phase lock loop circuit to a clock input of each JK flip-flop of a Johnson counter, the Johnson counter comprising N JK flip-flops including an input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops, each JK flip-flop having a J input, a K input, the clock input, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop;

generating the feedback signal in the Johnson counter in response to the output signal having the frequency $2NF_0$ from the phase lock loop circuit; and

generating an output clock signal from at least two of the N JK flip-flops of the Johnson counter, each output clock signal having a phase displaced from a phase of each other output clock signal by at least 360/2N°.

41. (Previously Presented) The method of claim 40 wherein N is 4.

42. (Previously Presented) The method of claim 40 wherein N is 8.

43. (Previously Presented) The method of claim 40, further comprising generating an output clock signal from each of the N JK flip-flops of the Johnson counter, the feedback signal being one of the output clock signals, the N output clock signals having a relative phase separation of at least 360°/2N and each output clock signal having a frequency F_0.

44. (Previously Presented) The method of claim 40, further comprising generating the feedback signal and each output clock signal with a frequency F_0.

45. (Previously Presented) The method of claim 40 wherein generating an output signal having a frequency $2NF_0$ comprises:

comparing the input clock signal having the frequency F_0 and the feedback signal and in a phase detector;

generating an output signal from the phase detector corresponding to a phase difference between the input clock signal having the frequency F_0 and the feedback signal;

generating a control signal in a low pass filter and a gain stage in response to the output signal from the phase detector; and

generating the output signal having the frequency $2NF_0$ in response to the control signal in a voltage controlled oscillator coupled to the low pass filter and the gain stage.

46. (Canceled)

47. (Previously Presented) The method of claim 40, further comprising:

generating an output clock signal from each Q output and each complemented Q output of each JK flip-flop of the Johnson counter, the 2N output clock signals having a relative phase separation of 360°/2N, and each output clock signal having a frequency F_0.

48. (Previously Presented) The method of claim 20 wherein N =8.